THE DESIGN AND FABRICATION OF A SILICON MEMBRANE FOR ELECTROSTATIC ACTUATION

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Keywords

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Abstract

THE DESIGN AND FABRICATION OF A SILICON MEMBRANE FOR ELECTROSTATIC ACTUATION

Elizabeth L. Brooks

An electrostatically actuated silicon membrane was designed and fabricated utilizing a silicon-on-insulator wafer. The SOI wafer contains three layers- a 400μm thick “handle” layer of silicon followed by a 2μm thick oxide layer topped with a 20μm thick “device” layer of silicon. The embedded oxide layer acts as an etch-stop during silicon etching, leaving a thin membrane of consistent thickness on the device side. The device dimensions were chosen to provide acceptable membrane deflection predicted by calculations and Finite Element Analysis. A microfabrication process plan was designed to produce thin membranes appropriate for electrostatic actuation. A 700nm layer of silicon dioxide was grown on both sides of the SOI wafer to be used as a mask during silicon etching. The handle side of the SOI wafer was coated with positive photo resist and the wafer was patterned through lithography using a measured light integral of 4. Following lithography, the exposed silicon dioxide on the handle side was etched with a buffered oxide etch, leaving regions of exposed silicon on the handle. The entire wafer was then placed in tetramethylammonium hydroxide at 85°C to etch through the 400μm of exposed silicon on the handle. Previous experiments with TMAH gave an average etch rate of 35μm/s for silicon. The TMAH etch was stopped by the imbedded layer of silicon dioxide, leaving the 22μm thick silicon membranes. Finally, the remaining silicon dioxide was removed with another buffered oxide etch. The final etch depth was measured with a profilometer.

Section 1: Introduction

1.1 Broader Impact

The World Health Organization estimated in 2001 that 250 million people worldwide have a disabling hearing impairment. Currently, one-tenth of the hearing aids needed globally are in existence; 75% of these are distributed to North America and Europe, 13% to Japan, Australia and New Zealand, and 12% to the rest of the world.[1] Typical hearing aids are generally too expensive for individuals in less developed countries (LDCs) and require unavailable education and energy sources. There is a pressing need for hearing aids that are affordable for individuals in LCDs, with consideration to their resources.

1.1.1 Prevalence of Hearing Loss in Less Developed Countries

Individuals in LDCs are twice as likely to develop a hearing impairment as an individual in a developed country due to of living conditions that contribute to hearing loss. Problems during pregnancy and childbirth including birth conditions, infectious diseases during pregnancy, misuse of ototoxic drugs, and jaundice can cause hearing impairment in a newborn baby. During childhood, infectious diseases such as meningitis, measles, mumps, and chronic ear infections can lead to hearing loss. Other risks include wax blockage, head injury, and excessive noise. Most of these risk factors are elevated in LDCs. Low-quality, inaccessible health care contributes to childbirth complications, infectious diseases, and poor health education. Preventative measures such as immunizations, monitored drug dosages, disease diagnosis, and treatment may not be available. Operating machinery without protective gear and noise control can expose individuals to dangerous levels of noise. Exposure to gunfire or explosions can also damage the ear and are experienced more in countries with weak government structures.[2]

Along with the increased risk, hearing impairment is stigmatized in LDCs due to poor health care and education. The development of a child's language and cognitive skills can be delayed due to the inability to hear correctly. Hearing-impaired adults are unlikely to adequately perform and keep their jobs. Without health care or special education programs, these individuals are often isolated and stigmatized.[2]

1.2 Improving Hearing Aids

A hearing aid has four basic parts: a microphone, amplifier, speaker, and battery. The microphone receives sound waves and converts them into electrical signals. The amplifier receives the electrical signals and increases their power. The speaker takes the amplified signals and converts them back into sound waves and into the ear.[3] The battery powers the microphone, amplifier, and speaker. A microspeaker alone accounts for 50-95% of the power consumption in a hearing aid.[4] Decreasing the consumption levels of the speaker will prolong operation life and decrease the dependence on the power source.

1.3 Electrostatic Actuation

Electrostatic actuation relies on differential voltage rather than current, allowing for low power consumption. The design is simple; it requires few materials and can be fabricated with basic microelectromechanical systems (MEMS) fabrication techniques. Electrostatic actuation provides a fast response due to the good charging and discharging time constants of conductors, enabling high frequency applications.[5] The compatibility with basic MEMS fabrication techniques can enable batch processing and lower production costs.

1.3.1 Electrostatically Actuated Microspeaker

An electrostatically actuated microspeaker functions as a capacitor with a conductive diaphragm and lower conductive plate (Figure 1.1). When a voltage is applied to the electrode plates, an

attractive electrostatic force develops. When this force overcomes the mechanical restoring force of the diaphragm, the diaphragm will deflect (Figure 1.1). The volume change of the air inside the cavity creates a pressure wave that can be transferred to the ear. This pressure difference can be measured by a MEMS pressure sensor for characterization. An oscillating differential voltage applied to the electrodes can be controlled to produce different sound waves. The electrostatic force is dependent upon the surface area of the electrodes, the distance between the electrodes, and the applied voltage.[6] Due to the fabrication capabilities of our lab, I am limited on larger distances between plates. To compensate, I will have to design the device with a relatively large surface area and large differential voltage. The maximum voltage was determined to be 200V because this could be achieved by a standard laboratory DC power supply.

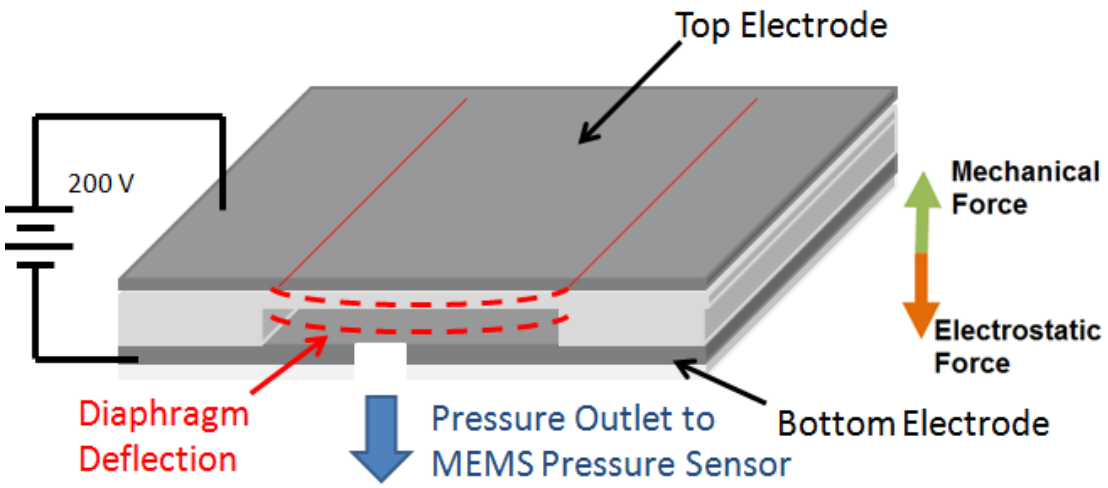

Figure 1.1: Electrostatically Actuated Diaphragm Model: An applied voltage creates an electrostatic force that causes the diaphragm to deflect. The deflection creates a pressure differential inside the cavity that can be sensed by a MEMS pressure sensor. 200V was chosen because it can be achieved with a standard laboratory DC power supply. The balance of forces is shown (right).

1.3.2 Previous Work Done at Cal Poly

Electrostatically actuated diaphragms have been researched, designed, and fabricated by Brian Stahl at Cal Poly. He attempted to fabricate diagrams by doping one side of a silicon wafer with boron to create an etch-stop for silicon etching. This led to significant warping in the diaphragms due to stress build-up that accumulated during processing. To prevent this problem, I fabricated my diaphragms with a silicon-on-insulator (SOI) wafer. For this first year of research, I fabricated my diaphragms with a mask made by Brian Stahl that produced diaphragms of five different sizes. This enabled me to investigate the warping of my processing as a function of diaphragm size. If size did have an impact on warping, I could change my own design and prevent warping for my actual devices.

Section 2: Design

2.1 Summary

This section will outline the process that was used to design the device. Initially, steady-state algebraic equations were used to predict the membrane displacement based on dimensions and applied voltages. These equations were modified to consider the increase in electrostatic force that occurs as the distance between the plates decreases while the membrane deflects. Necessary design constraints were added to ensure proper functioning of the device. Once appropriate dimensions were selected, the device was modeled with SolidWorks for finite element analysis.

2.2 Diaphragm Mechanics

The mechanics of square membranes was examined to estimate the deflection of the diaphragm and ensure that the stresses produced by actuation would not lead to device failure.

An ideal membrane can be considered a square plate of uniform thickness fixed at all four edges. The plate is assumed to be in pure bending due to the high aspect ratio of the diaphragm. The flexure rigidity *D* of the diaphragm is calculated with Equation (2.1):

$$D = \frac{Eh^3}{12(1-\nu^2)} \tag{2.1}$$

where *E* is Young's modulus, *h* is the membrane thickness, and *v* is Poisson's ratio. The deflection (*w*) at any point can then be calculated:

$$\omega(x,y) = 0.0213p\frac{a^4}{D}\left(1-\frac{x^2}{a^2}\right)^2\left(1-\frac{y^2}{a^2}\right)^2 \tag{2.2}$$

where x and y are points that deviate from the center of the square diaphragm (Figure 2.1), *p* is the uniformly applied pressure, and *a* is one-half the side length.

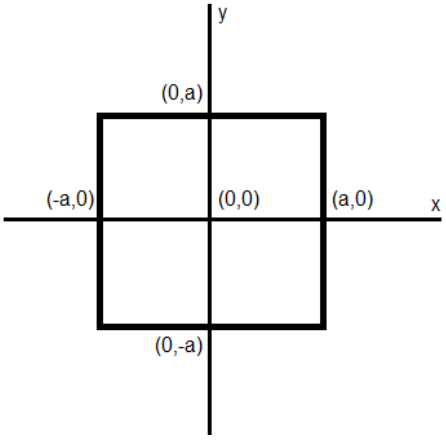

Figure 2.1: Coordinate System used with Equations (2.2) and (2.3)

As expected, Equation 2.2 shows that the maximum deflection occurs at the center of the diaphragm. The normal stress in the membrane σ_{xx} at any given point is calculated with Equation (2.3).

$$\sigma_{xx} = -0.51\frac{a^2}{h^2}\left[\left(1-\frac{x^2}{a^2}\right)^2\left(1-\frac{3y^2}{a^2}\right)+\nu\left(1-\frac{y^2}{a^2}\right)^2\left(1-\frac{3x^2}{a^2}\right)\right] \quad (2.3)$$

It is evident from Equation (2.3) that the maximum stress in the diaphragm occurs at the center of the edges of the diaphragm, at (±a,0) and (0, ±a) on Figure (2.1). Equations (2.2) and (2.3) estimate the stresses and deflection expected for a plate loaded by uniform pressure.[6]

2.3 Electrostatic Force

The diaphragm deflection is determined by the electrostatic force that develops between the two plates. The electrostatic force forms due to the separation of opposite charges concentrated on opposing plates. If the diaphragm and counterelectrode are treated as parallel plates fixed by two fixed-guided beams, the static capacitance C_o is given by

$$C_o = \frac{\varepsilon\varepsilon_o A}{d} \quad (2.4)$$

where ε is the permittivity of the dielectric medium between the two plates, ε_o is the permittivity of free space (ε_o = 8.854*10^{-12} F/m), A is the overlapping area of the plates, and d is the distance between the two plates. When a voltage V is applied to the plates, the attractive electrostatic force F_{elec} is estimated by

$$F_{elec} = \frac{C_o V^2}{2d} \quad (2.5)$$

Combining Equations (2.4) and (2.5) gives an equation for the electrostatic force between parallel plates in terms of membrane material properties and device dimensions:

$$F = \frac{\varepsilon\varepsilon_o A V^2}{2d^2} \quad (2.6)$$

2.4 Parallel Plate Actuation with Uniform Force

The applied equations assume that the electrostatic force is uniformly applied across the plates and that the plates do not deform. In reality, the diaphragm deforms toward the counterelectrode and the electrostatic force increases toward the center of the diaphragm where the gap distance between the plates is the smallest. The following approximations are based on a diaphragm deflection on the order of tens of microns, which is appropriate for this application.

The maximum deflection w_{max} at the center of the membrane can be found by combining Equations (2.1) and (2.2) at the center of the diaphragm:

$$w_{max} = 0.015975p\frac{(1-\nu^2)L^4}{Eh^3} \tag{2.7}$$

where L is the side length (L=2a). To find the maximum deflection in terms of the electrostatic force, replace p with F/L^2. This assumes a constant force.

$$w_{max} = 0.015975\frac{(1-\nu^2)F_{elec}L^2}{Eh^3} \tag{2.8}$$

Combining Equation (2.8) with Equation (2.6) gives the maximum deflection in terms of the membrane's material properties, device dimensions, and applied voltage:

$$w_{max} = 0.015975\frac{(1-\nu^2)\varepsilon\varepsilon_0 A^2V^2}{2Ed^2h^3} \tag{2.9}$$

2.5 Accounting for Nonlinear Force Response

Equation (2.9) serves as a rough approximation for diaphragm deflection and does not account for the nonlinear electrostatic force response. As the diaphragm deflects closer to the counterelectrode, the electrostatic force increases with decreasing gap distances. As previously stated, the electrostatic force is balanced by the mechanical restoring force of the diaphragm. If the membrane is treated as a simple spring, Hooke's law gives the mechanical restoring force F_{res} as:

$$F_{res} = kx$$

(2.10)

where *k* is the effective spring constant of the diaphragm and *x* is the diaphragm displacement. The displacement can be defined as:

$$x = d_o - d \tag{2.11}$$

where d_o is the gap distance between the plates before actuation and *d* is the gap distance after actuation. At equilibrium, the mechanical restoring force is equal to the electrostatic force (Equation (2.12).

$$F = F_{elec} + F_{res} = 0 \tag{2.12}$$

The balanced load displacement can be found by combining Equations (2.6), (2.10), (2.11), and (2.1):

$$0 = \frac{\varepsilon\varepsilon_o A V^2}{2(d_o - x)^2} - k(d_o - d) \tag{2.13}$$

where $A=L^2$ for the square diaphragm. This equation accounts for the increasing electrostatic force with displacement, but it still assumes a rigid plate with uniform deflection toward the membrane. In reality, the sides of the diaphragm are fixed at the edges, so the deflection varies from little deflection near the sides to the largest deflection at the center. The approximation made for Equation (2.13) becomes less valid as the deformation becomes greater. At small deformations the membrane is closer to plate-like.

The effective spring constant of the membrane, *k* can be found by using Equation (2.8) and solving for the force divided by the maximum deflection:

$$k = \frac{F_{elec}}{w_{max}} = \frac{Eh^3}{0.015975(1-\nu^2)L^2} \tag{2.14}$$

This spring constant can replace the spring constant in Equation (2.13):

$$\frac{Eh^3(d_o-d)}{0.015975(1-\nu^2)} = \frac{\varepsilon\varepsilon_o L^4 V^2}{2d^2} \quad (2.15)$$

From this equation the deflection of the diaphragm *d* can be calculated with diaphragm dimensions, applied voltage, and material properties.

2.6 Electrostatic Actuation Concerns

2.6.1 Pull-In Voltage

The upper limit of applied voltage for electrostatic actuation is the breakdown voltage predicted by Paschen's Curve (Figure 2.2). As the distance between the two electrodes decreases, the electrostatic force increases nonlinearly. With an increasing applied voltage, the electrostatic force curve increases ($V_4>V_3>V_2>V_1$ on Figure 2.2). At the pull-in voltage, the electrostatic force over-exceeds the mechanical restoring so that that deflection of the membrane cannot balance the forces. The top electrode deflects so far that it hits the bottom electrode and sticks, resulting in snap-down. At the pull-in voltage, the electrostatic force becomes tangential to the mechanical restoring force, indicating that any voltage at or above this voltage will prevent equilibrium between the two forces. Staying below this pull-in voltage will prevent snap-down.

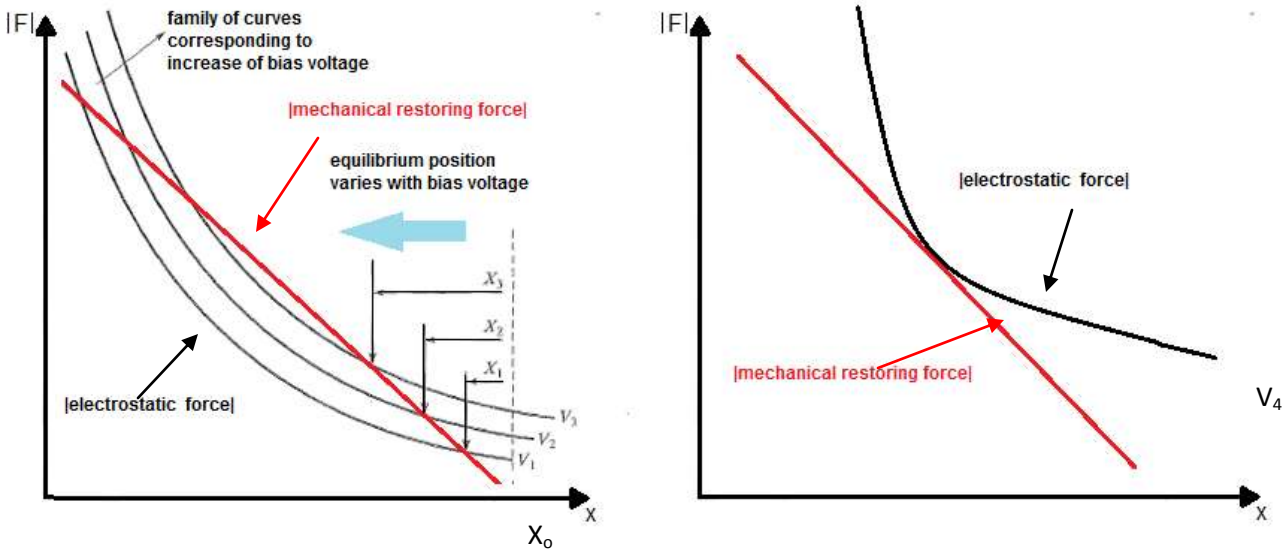

Figure 2.2: Paschan's Curve: The mechanical restoring force and electrostatic force graphed as a function of the distance between the plates, x. At higher voltages, the electrostatic force curve rises. The intersection points between the two curves are equilibrium points (left). The voltage at which the mechanical restoring force lies tangentially to the electrostatic force (right) is the pull-in voltage, V_4. Above this voltage, equilibrium does not exist and snap-down occurs.[5]

The pull-in voltage V_p can be found by taking the derivative of Equation (2.13) with respect to x:

$$0 > \frac{\varepsilon\varepsilon_o A V^2}{(d_o - x)^3} - k \qquad (2.16)$$

Equation (2.13) can be further manipulated:

$$0 > x\frac{\varepsilon\varepsilon_o A V^2}{(d_o - x)^3} - \frac{\varepsilon\varepsilon_o A V^2}{2(d_o - x)^2} \qquad (2.17)$$

Solving Equation (2.17) for x gives the critical displacement x_c:

$$x_c = \frac{d_o}{3} \qquad (2.18)$$

This shows that the membrane cannot deflect more than a third of the gap distance, otherwise snap-down will occur. This model should provide a generous measurement, because the added support of a four-sided diaphragm should increase the mechanical restoring force and allow for a higher pull-in voltage. The pull-in effect can be eliminated with a series capacitor, but a much

higher operation voltage is required to support the two capacitors.[6] Substituting the critical displacement for the displacement in Equation (2.14) gives an equation of critical design parameters:

$$\frac{8}{27}d_o^2 = \frac{0.015975\varepsilon\varepsilon_o(1-\nu^2)V^2L^4}{Eh^3} \quad (2.19)$$

2.6.2 Fringe Effects

Fringe capacitance along the edges of the diaphragm can alter the electrostatic force attraction.[5] For this device, the side lengths of the plates are much larger than the spacing between them, so fringe effects can be ignored.[6]

2.6.3 Breakdown Voltage

Paschen's law states the breakdown voltage between parallel plates separated by a gas as a function of operating pressure *p,* and electrode gap distance, *d*:[7]

$$V_b = \frac{A(pd)}{\ln(pd)+B} \quad (2.20)$$

Where *A* and *B* are experimentally obtained constants dependent upon the gas medium. For air, *A* is 15 $cm^{-1}Torr^{-1}$ and *B* is 365 $V*Torr*cm^{-1}$. This breakdown voltage needs to be avoided to prevent electron ionization between the electrodes.

2.7 Design Constraints

Design constraints were applied to eliminate variables and reduce the design to the geometry of the diaphragm.

2.7.1 Applied Voltage

As previously stated, the gap distance between the plates is constrained to larger distances due to microfabrication processing. To get a deflection high enough to be measured by a MEMS pressure sensor, a large voltage and large plate area was used for this research. The maximum voltage was chosen to be 200V because this could be generated with a laboratory DC power supply.

2.7.2 Material Selection

Materials for different parts of the device were selected based on design requirements and fabrication capabilities (Figure 2.3). Silicon was chosen for the diaphragm material because it can be etched to achieve a small diaphragm thickness. Silicon wafers are compatible with our microfabrication equipment and is the most widely used substrate in MEMS design.[8] Silicon is ideal for the following reasons:

1. It is mechanically stable.
2. Electronics can be integrated onto the same substrate.
3. It has a high Young's modulus, about the same as steel (1.5×10^5 MPa). This allows for fast actuation times with an oscillating voltage.
4. It is very light, about the same mass density as aluminum (2.3 g/cm^3).
5. It has a high melting temperature at 1400°C. The silicon can easily withstand oxidation processing temperatures of 1050°C.
6. The coefficient of thermal expansion is small compared to comparable materials (steel or aluminum). This is important because the coefficient of thermal expansion of silicon dioxide is very small. Silicon dioxide is used as a masking layer and etch stop in the fabrication process. If the difference of coefficients was great between the silicon and

silicon dioxide, the cooling after oxidation would create stresses between the layers. These stresses may cause warping in the final thin membrane of the device.

The bottom of the device will be made of Pyrex, a borosilicate glass. Pyrex was chosen because it is transparent, allowing accurate alignment between the top and bottom structure. It can be masked and sputtered with gold to create a conductive counterelectrode. It can be etched with a reactive ion etcher to decrease the gap size between the two plates. The silicon diaphragm and Pyrex wafer will be bonded together with SU-8, a photo-definable epoxy based polymer. SU-8 can be spin-coated to a 50 micron thickness and then cured with applied heat and pressure to seal the cavity. This will be the material of the side walls of the cavity.

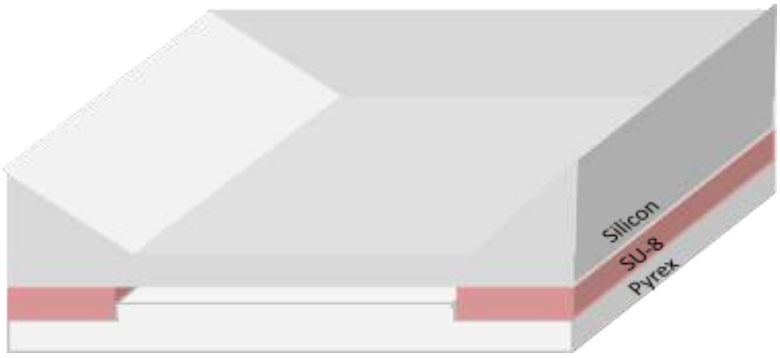

Figure 3.3: Materials Selection for Microspeaker: The diaphragm is silicon, the bottom plate is Pyrex, and the walls are SU-8.

2.7.3 Maximum Plate Area

The electrostatic force increases proportional to the plate area (Equation 2.6). To maximize the electrostatic force, the plate area needs to be maximized.

2.7.4 Minimum Measurable Deflection

The approximate change of pressure in the cavity can be found by treating the air in the cavity as an ideal gas and the cavity as a closed system. The ideal gas law gives:

$$P_1 V_1 = P_2 V_2 \tag{2.21}$$

where P_1 is atmospheric pressure (101.325 kPa), V_1 is the initial volume of the cavity, P_2 is the final pressure and V_2 is the final volume. For further simplification, the plate can be assumed to have flat, plate-like deformation. This reduces the volume geometry to cubes. Substituting for the volumes gives Equation (2.22):

$$P_1 d_o lw = P_2 d_2 lw \tag{2.22}$$

where d_o is the original distance between the plates, d_2 is the distance between the plates after deflection, l is the length, and w is the width of the cavity. Only the height is changing with diaphragm deflection, so Equation (2.22) can be further simplified:

$$P_1 d_o = P_2 d_2 \tag{2.23}$$

We are actually trying to measure a difference in pressure, so Equation (2.23) can be changed to:

$$P_1 d_o = (P_1 + P)(d_o + d) \tag{2.24}$$

Where P is the change in pressure and d is the deflection. The change in pressure must be larger than the pressure sensitivity of a MEMS microphone to be able to be sensed for characterization. A typical MEMS sensor can sense 0-37kPa.[9]

2.7.5 Minimum Gap Distance

The electrostatic force between electrodes increases with smaller gap distances (Equation 2.6). The SU-8 used to fabricate the side-walls of the diaphragm can be applied at a 50μm thickness. This will be the maximum gap distance used for design purposes. A minimum realistic gap distance that can be achieved by additional etching is 10μm.

2.8 Concerns with Design Equations

The calculations performed thus far are simplified estimates. Accurate solutions are complicated problems that can only be solved through Finite Element Analysis. A SolidWorks model was produced to provide better conceptual modeling.

2.9 Final Dimensions

The final dimensions of the device were extracted beginning with the minimum required deflection that a MEMS pressure sensor can measure (Equation 2.24). The initial pressure inside the cavity was assumed to be atmospheric pressure, 101.325 kPa. The initial height was based on the minimum realistic distance that could be fabricated between plates- 10μm. The change in pressure that could be measured by a MEMS pressure sensor was assumed to be 25kPa. With these given values, a required deflection of 2.5μm was estimated (roughly) to be the deflection needed for diaphragm actuation. This deflection is less than a third of the distance between the plates, so snap-down should not occur (Equation 2.18).

Next, Equation (2.15) was used to approximate an appropriate side length for the electrode plates. Young's modulus of single crystalline (100) silicon is 1.5×10^{11}Pa and Poisson's ratio is 0.22. The applied voltage was 200V and the thickness of the diaphragm that could be achieved with an SOI wafer was 10μm. With these predictions, an approximate side length of 1.2 mm was determined to be sufficient for actuation. The device with these dimensions (Figure 2.4) was then ready for modeling.

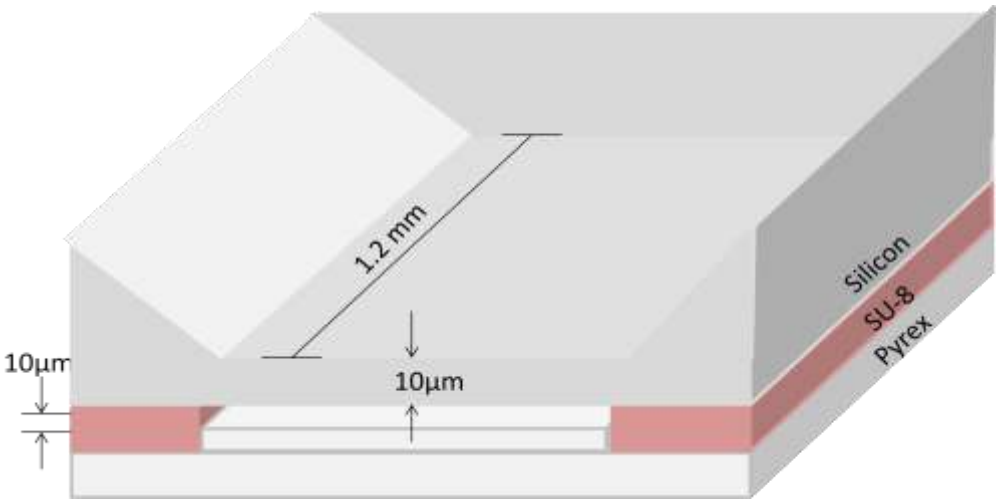

Figure 4.4: Final Dimensions of the Diaphragm

2.10 Modeling

The device was modeled in SolidWorks (Figure 2.5) to ensure that stresses in the diaphragm due to actuation would not lead to fracture. SolidWorks gave a maximum stress in the diaphragm of 1.4MPa, far below the tensile strength of silicon, 120MPa.

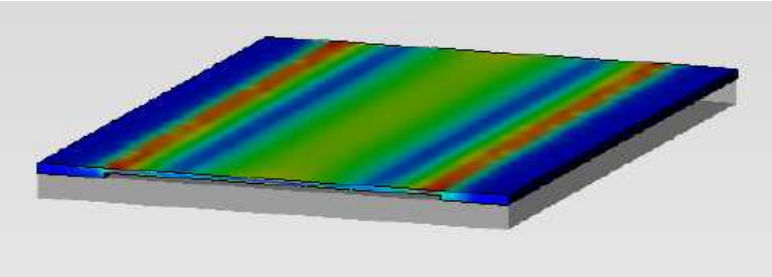

Figure 5.5: SolidWorks Model of the Device: The device was modeled as a cross section for simplification. The maximum stress in the diaphragm occurs at the edges (red area).

Section 3: Fabrication

3.1 Summary

The goal for this first year of research was to fabricate silicon diaphragms. Silicon-on-insulator (SOI) wafers were chosen to provide an etch stop for silicon etching. The wafers were oxidized and patterned to create etch windows. A mask created by Brian Stahl produced sixty diaphragms of five different sizes. They were then anisotropically etched with tetramethylammonium hydroxide (TMAH), before stopping at the embedded oxide layer. Finally they were inspected and the etch depth was measured with a profilometer.

3.2 Wafer Selection

The substrate selection is extremely important in MEMS design because the processing steps are highly dependent upon the particular crystallographic orientation and defect/impurity concentration. The crystallographic geometry especially influences silicon wet etching. The wafer must be polished on both sides with a low thickness variation to etch multiple uniform membranes. If the thickness of the substrate varies, so too will the membrane thicknesses. An SOI wafer was required to provide an etch stop that would allow multiple uniform membranes. Previous research done by Brian Stahl looked at doping a silicon substrate to create an etch-stop. Unfortunately, this created internal stresses in the membranes that caused warping.

SOI wafers are typically used in MEMS design to prevent charge leakage between p-n junctions.[11] I will be using one to fabricate membranes with the embedded oxide layer as an etch-stop. The wafer is a double-side polished, 100mm (diameter) SOI prime silicon wafer. The crystal orientation is <100> ± 0.5°. This orientation was chosen because it provides a flat bottom parallel to the surface for membrane fabrication (Figure 3.1).

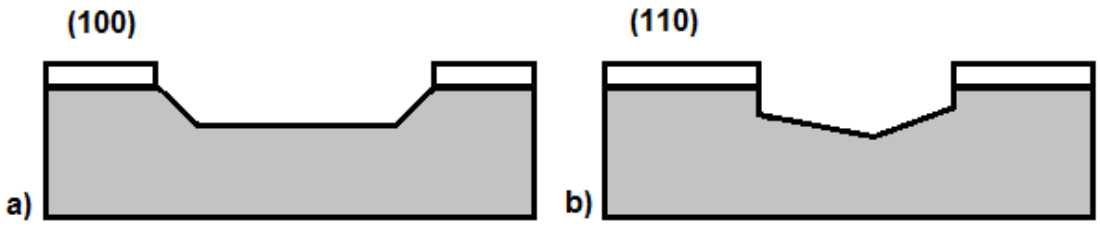

Figure 3.1: Anisotropic Silicon Etching a) anisotropic silicon etching of a (100) wafer b) anisotropic silicon etching of a (110) wafer.

The SOI wafer has three layers; a 400 ± 10μm thick handle layer, a 2 ± 0.10μm thick embedded oxide layer, and a 20 ± 1μm thick device layer (Figure 3.2). I will be etching through the wafer handle, so the critical tolerance is with the N-type silicon device layer that will be the thin membrane. The thickness variation for the device layer (1 μm) is much less than the overall thickness of the diaphragm (20 μm).

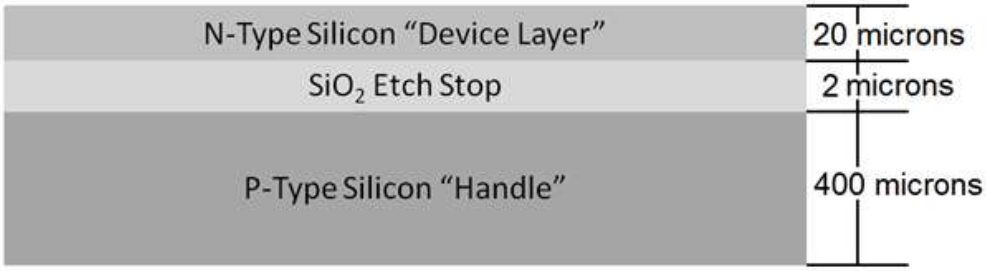

Figure 3.2: Silicon-on-Insulator Wafer Cross Section

3.3 Wet Thermal Oxidation

An oxide layer was grown on both sides of the wafer to provide an etch mask during silicon etching (Figure 3.3). The oxide layer was patterned using lithography on the handle side of the wafer to create etch windows. The device layer remained covered by the oxide until silicon etching was complete. Thermally grown oxides are commonly used as mask material because

they have a very low etch rate in silicon etchants. A thick oxide of 8000Å was chosen as a target to provide more than enough protection during etching and processing. Oxides over 1µm thick can create bowing in the wafer, so it is recommended to use oxides thinner than 1µm.[8]

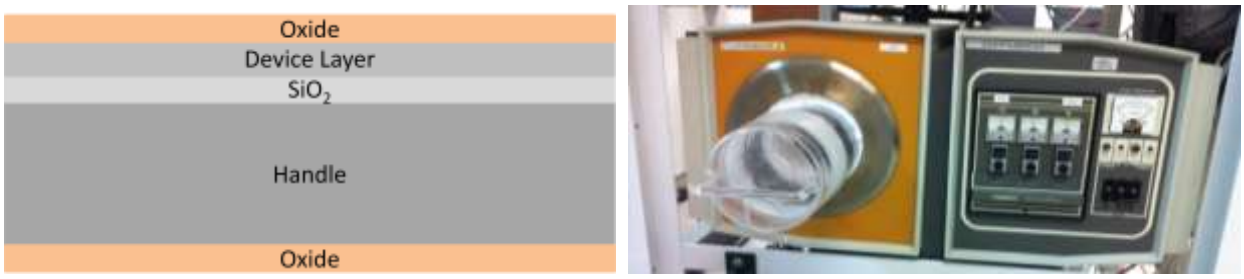

Figure 3.3: Wet Thermal Oxidation: Wafer cross section after oxidation (left) and the oxidation tube furnace (right)

3.3.1 Wet Oxidation vs Dry Oxidation

The oxide was grown thermally in an oxidation furnace through wet oxidation. Wet oxidation introduces water vapor into the furnace at high temperatures (1050°C). The water reacts with the silicon to create silicon dioxide on the surface of the silicon, and dihydrogen gas.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

The thermally grown oxidation layer has a different molecular volume and coefficient of thermal expansion than the silicon substrate. The oxide layer is under compression, causing significant stress between the oxide layer and the substrate. Wet oxidation reduces these compressive stresses and speeds up the oxide growth. Dry oxidation would take longer, but provide a better quality oxide layer with virtually no pin-holes.[8] I lost many devices to pin-hole etching, so dry oxidation should be considered in the future. Oxidation takes less time with wet oxidation because a water molecule is much smaller molecule than O_2, so diffusion occurs much faster. Water also loosens the SiO_2 structure during oxidation, making it easier for a diffusing species.[8]

3.3.2 Estimating Oxidation Time

The Deal-Grove model predicts the oxide thickness x_0 based on the oxidation environment:[10]

$$\frac{x_0}{\frac{A}{2}} = \left[1 + \frac{t+\tau}{\frac{A^2}{4B}}\right]^{1/2} - 1 \qquad (3.1)$$

where A for wet oxidation at 1050°C is 0.292μm and B is 0.35μm^2/hr, t is the oxidation time in hours, and τ is a factor that accounts for silicon's native oxide. At relatively long times, t>>A^2/4B, t>>τ and the equation can be reduced to:

$$x_0 \cong \sqrt{Bt} \qquad (3.2)$$

With Equation (3.2) it is predicted that a two hour oxidation period at 1050°C will produce an 8000Å oxide thin film.

3.3.4 Oxidation Process

Before thermal oxidation, the device wafers and two "dummy wafers" were cleaned in Piranha at 70°C to remove organics and dipped in a buffered oxide etchant (BOE) for 5 minute to remove oxides. The dummy wafers were two p-type silicon wafers that were placed on either side of the SOI wafer in the furnace to minimize turbulent gas flow around the SOI wafer. The oxidation tube furnace was first preheated to 900°C. Once 900°C was reached, ultra-high-purity (UHP) nitrogen was turned on at a 5 L/min flow rate. The SOI wafer surrounded by the dummy wafers were placed in a quartz boat and loaded into the furnace at about 0.5 cm/second to prevent thermal shock. The temperature was then increased to 1050°C while the UHP Nitrogen prevented oxidation during the warm-up. Once the desired oxidation temperature 1050°C was reached, the nitrogen was stopped and UHP oxygen was turned on at a 5 L/min flow rate. The oxygen was bubbled through boiling water to produce a water vapor for wet oxidation. The wet oxidation was carried out for two hours. After two hours, the furnace and UHP oxygen were turned off, and UHP nitrogen was switched back on at 5 L/min. As the furnace cooled to 900°C,

the UHP nitrogen prevented further oxidation. When the furnace reached 900°C, the UHP nitrogen was turned off and the furnace was allowed to cool overnight. Once at room temperature (RT), the quartz boat was removed. The oxidation process is summarized in Table (3.1).

Table 3.1: Oxidation Process Steps for an 8000Å Oxide Film

Process Step	**Temperature**	**Gas**
Pre-heat furnace	RT to 900°C	None
Insert Wafers	900°C	UHP N_2 at 5 L/min
Warm-up	900°C to 1050°C	UHP N_2 at 5 L/min
Oxidation for 2 hours	1050°C	Wet UHP O_2 at 5 L/min
Cool-down	1050°C to 900°C	UHP N_2 at 5 L/min
Cool-down	900°C to RT	None
Remove Wafers	RT	None

3.3.5 Measuring the Oxide

After the wafers were removed from the furnace, a Filmetrics F20 thin-film measurement system was used to measure the oxide thickness on the back and front of the wafers. Each side was measured in five different places, with a mean of about 9500Å on each side. This is considerably more than predicted by the Deal-Groove model. A smaller oxide layer is recommended for future fabrication processes because 9.5 μm is very close to the 1μm oxide layer that is known to create wafer bowing.[8]

3.4 Lithography

After oxide measurements, the SOI wafer was cleaned again in 70°C Piranha for 10 minute and 25°C BOE for 5 minute before lithography. The wafers were spin-rinsed and dried with low-purity (LP) nitrogen.

The SOI wafer was first baked at 150°C for 5 minute to remove any solvents or water left over from the cleaning process. The wafer was then placed on a Laurell Technologies WS-400B-

6NPP spin-coater with the handle side facing up and held with a vacuum chuck. 2.5mL of Microchem MCC Primer 80/40 was applied to the wafer to promote adhesion between the resist and wafer. The wafer was spun at 3000 RPM for 30 seconds. Next, 5 mL of Rohm-Haas Microposit s1813 positive photoresist was dispensed into the center of the wafer in a continuous stream. The wafer was spun at 500RPM for 10 sec, 4000RPM for 20 sec, and 300RPM for 5 sec. The first spin step spread the photoresist over the wafer surface, the second planarized the photoresist, and the last step brought the wafer to a gradual stop (Table 3.2). The wafer was removed from the spin-coater and soft-baked on a hot-plate at 90°C for 1 minute to drive off solvents, reduce stresses, and promote adhesion between the resist and wafer.[8]

Table 3.2: Spin Coating Steps: used for positive photoresist application

Step #	Speed (RPM)	Time (seconds)	Purpose
1	300	30	Spread primer over wafer surface
2	3000	30	Planarized primer
3	3000 to 200	20	Slow wafer, pause during this step to apply resist
4	200 to 500	10	Spread resist over wafer surface
5	4000	20	Planarized resist
6	4000 to 300	5	Slow to stop

The wafer was then placed in a Canon PLA-501FA aligner for mask alignment and exposure. A light integral of 4 was used, corresponding to a 15 second exposure time with a 150mJ/cm^2 exposure dose. A diaphragm mask created by Brian Stahl was aligned to the wafer and the wafer coated with resist was exposed by a mercury arc lamb. The exposed positive photoresist was weakened by rupture or scission of the main and side polymer chains, making it more soluble in developer.[8] The wafer was placed in Rohm Hass CD-26 positive resist developer for 2 minutes at room temperature. This left the unexposed photoresist in the pattern determined by the mask. The wafer was then inspected to ensure proper pattern transfer.

Finally the wafer was hard baked for one minute at 150°C to drive off any remaining solvents and ensure that the reactions initiated by exposure had run to completion.[8] A cross section of the device at this point is shown in Figure (3.4).

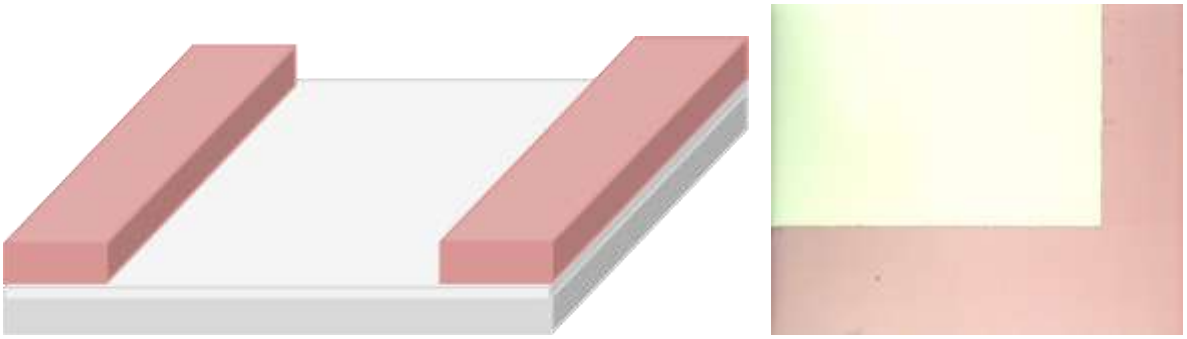

Figure 3.4: Device Wafer after Lithography: On the left is a cross-sectional model. The grey layer is the SOI wafer, the white layer is the top oxide (facing the wafer handle), and the pink layer is the patterned photoresist. On the right is a micrograph. There is a clear definition of photoresist (pink) and oxide.

After patterning, the exposed oxide was etched on the handle side with BOE for 10 minute at room temperature. This was accomplished using a single-sided etching apparatus (Figure 3.5). After etching, the wafer was rinsed with DI water, and submerged in 1500mL of Shipley Microposit Remover 1165 at 60°C for ten minutes to remove the photoresist. The device cross-section at this point is shown in Figure (3.6).

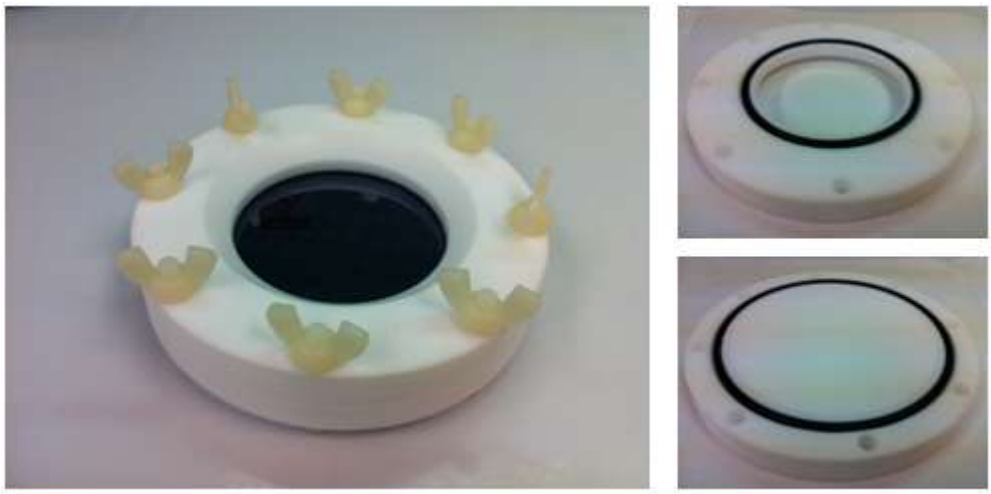

Figure 3.5: Single-Sided Etcher: The single-sided etcher has two o-rings that seal the wafer between two Teflon (white) wafer holders. Full assembly with BOE is shown (left), and the two halves of the etcher before assembly are shown (right).

Figure 3.6: Wafer Cross-Section after BOE Etch: The oxide layer (white) has been etched in a buffered oxide etchant (BOE). The photoresist has been removed, leaving exposed silicon (grey) etch windows.

3.5 Anisotropic Wet Etching

The diaphragms were created by etching silicon with tetramethylammonium hydroxide (TMAH). The SOI wafer was covered with a continuous oxide on the device side and a patterned oxide on the handle. The embedded oxide layer in the SOI wafer is positioned 20μm away from the device side. To create the thin membrane, I etched through the 400μm of silicon on the handle until the embedded oxide was reached.

TMAH's etch rate increases with decreasing TMAH concentration. To keep the concentration constant, the etching was done in a condenser chamber to prevent evaporation during etching. The etching chamber (Figure 3.7) has a two water cooling lines that condense and redeposit any evaporated chemical back into the solution. The lid is secured tightly with screws and an o-ring. Two thermocouples access the solution through a glass vent tube; one thermocouple goes to the resistive heating wrap and one goes to a thermometer. The foil wrap heater is controlled by an Omega temperature controller and regulates the temperature of the bulk of the solution. To achieve a stable etching temperature of 85°C, the hot plate was set to 130°C and the foil wrap heater was set to 85°C. A stir rod was used at a stir speed of 1 to reduce the formation of bubbles or areas of concentrated etchant.

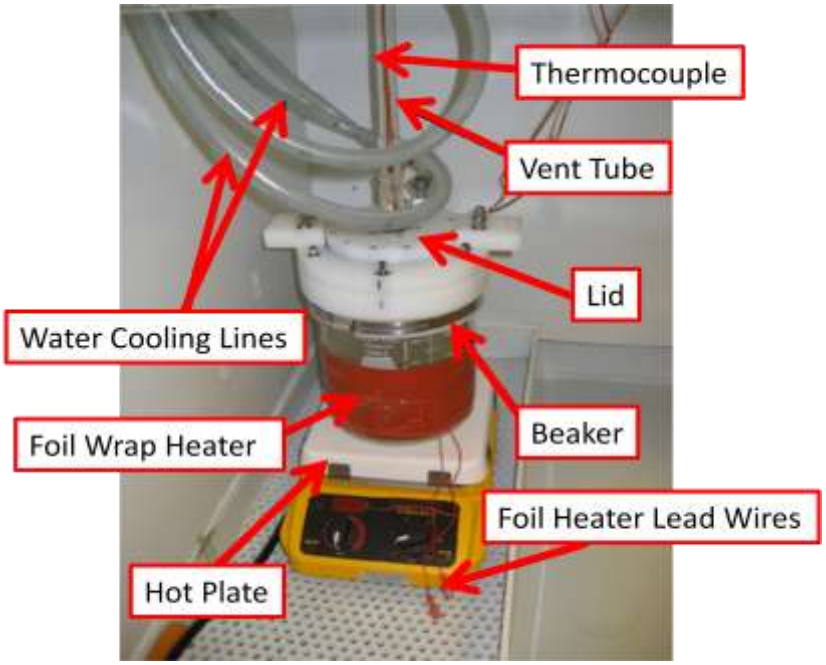

Figure 3.7: Condenser Chamber Diagram: This condenser chamber was created in our lab at Cal Poly. It is widely used for deep etching but is somewhat unpredictable.

TMAHW (tetramethylammonium hydroxide, water) was chosen as the chemical for wet etching silicon. THAHW does not decompose below 130°, is nontoxic, relatively inexpensive, and easily handled.[8] TMAHW in low concentrations etches faster, but often leaves hillocks and rough

surfaces. A TMAH concentration of 25 wt% was chosen because this was the concentration that the solution came in, and therefore was the maximum concentration I could work with. A higher concentration would also provide a less sensitive etch stop time.

The reactant transportation rate is dominated by diffusion and can be increased by solution agitation. Stirring the solution can also eliminate bubbles and regions of accumulated reactants. The surface reaction rate is most influenced by the temperature, etched material, and etchant concentration. The reaction sequence is as follows:[12]

$$Si + 2OH^- + 2H_2O \rightarrow Si(OH)_2^{2-} + 2H_2$$

3.8 Device Characterization

Sixty silicon diaphragms of five different sizes were produced. After fabrication, the devices were inspected and measured to ensure that the proper diaphragm thickness had been achieved.

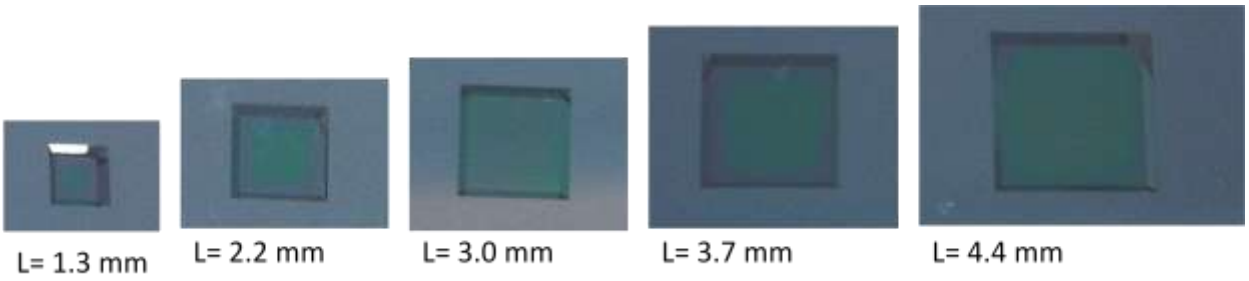

Figure 3.8: Different Size diaphragms produced: L is the side length of each square diaphragm

3.8.1 Yield

72% of the diaphragms were without holes or warping. A few of the larger diaphragms (1.2cm side length) exhibited slight warping, but was barely noticeable to the eye. For the continuation of my research, I will use diaphragm sizes smaller than the 1.2cm side length diaphragms to

completely avoid warping. The diaphragm size from my model was 1.2mm, slightly smaller than the smallest diaphragm I fabricated.

3.8.2 Profilometry

The etch depth of the cavities were verified with a stylus profilometer. Twenty diaphragms were measured and all had etch depths of around 400μm, indicating that the diaphragms are around 20μm thick (Figure 3.9). It should be noted that the maximum measurement capacity of our profilometer is 400μm, so this measurement tool would not be useful for measuring a larger etch depth.

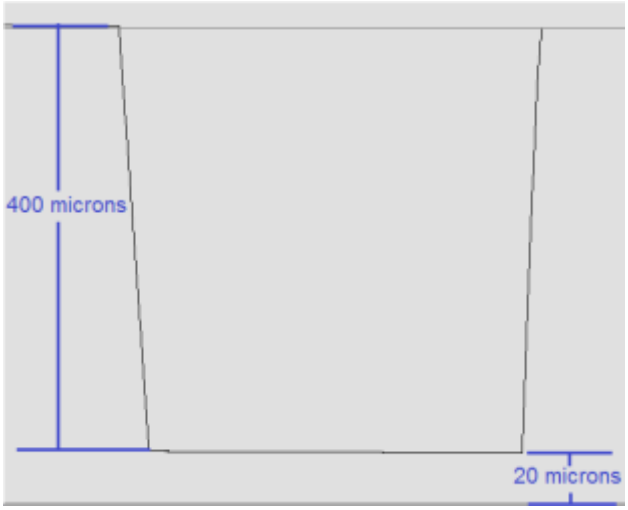

Figure 3.9: Etch Profile of a Diaphragm: The blue reference lines indicate the 100μm etch depth and 20μm diaphragm thickness. The sloping silicon etch profile is a consequence of the crystallographic planes.

Section 4: Discussion

4.1 Device Failure

Device failure was mainly caused by small etched holes in the diaphragms (Figure 4.1). This could have been the result of a loose oxide structure produced by wet oxidation. Wet etching is known to create low density oxides prone to pin-holes. This pin-hole could have allowed etching through the small hole, resulting in the square-etched holes characteristic of silicon etching.

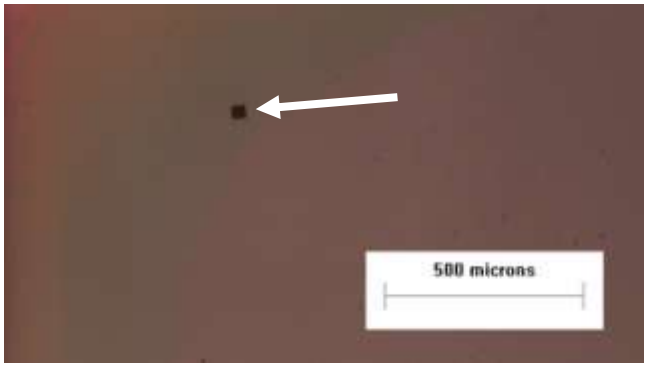

Figure 4.1: Holes in Diaphragm: The marked hole is about 32μm by 32μm large.

4.2 Future Fabrication Steps

The rest of the device will be fabricated next year for the completion of my Master's Thesis. The diaphragms will need to be fabricated again with proper dimensions and using an SOI wafer with a 10μm thick device layer. The bottom half of the device will be made of Pyrex and sputtered with gold to create electrical contacts. The bottom half will be bonded to the top half with SU-8 to complete the device. If the cavity is sealed, a small hole will be drilled or etched into the bottom of the glass to provide a pressure outlet. The device will then be actuated and characterized with a MEMS pressure sensor.

Section 5: Conclusions

A theoretical analysis of membrane mechanics and finite element analysis provided a device design that can be characterized in our lab. I was able to fabricate thin silicon diaphragms of 20μm thickness with an SOI wafer. The wafer was oxidized and patterned to create etch windows on the side opposite the embedded insulation layer. Wet oxidation produced a thicker oxide layer than expected. A thinner layer should be used in future processing. The embedded oxide layer of the SOI wafer provided an etch-stop that significantly reduced the etch rate of silicon in TMAH. Most of the diaphragms (72%) were fabricated successfully. The rest had small etched holes through the thin silicon membrane. These holes are probably due to a poor oxide layer formed by wet oxidation.

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